## REMARKS/ARGUMENTS

Applicants received the Office action dated March 31, 2004, in which the Examiner rejected claims 1-16 as obvious over Gibson (U.S. Pat. No. 6,601,167). In this Response, Applicants amend claims 1 and 6. Based on the amendments and arguments contained herein, Applicants respectfully submit that all pending claims are in condition for allowance.

Gibson generally discloses using a "sequential access memory" to store boot code instead of a conventional read only memory ("ROM"). Gibson notes that in sequential memories "individual addresses are not accessible directly" and thus "it is necessary to read out an entire page or half page in order to obtain the code stored at any particular address on the page." Col. 1, lines 39-43. However, because sequential access memory is "lower in cost and higher in storage density than a random access memory," Gibson teaches using sequential memory in place of a ROM for storing a computer system's boot code. See col. 2, lines 17-21. Gibson discloses implementing the sequential access memory as a ROM, specifically an electrically erasable programmable ROM ("EEPROM"). Col. 3, lines 21-27. Column 2, lines 17-43 summarizes Gibson's contribution as follows:

> In view of the above, the present invention provides a computer system in which initial program execution is performed using only a sequential access memory, thereby eliminating the need for a separate non-volatile random access memory.
>
> This is achieved in a computer system according to the present invention, which includes a processor, a sequential access memory having a boot program stored therein, and a boot loader. The boot loader includes a state machine, which in response to initialization of the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program. The first portion of the boot code is created with the understanding that the sequential memory can only deliver sequential words of memory to the processor. The first portion of the boot code instructs the processor to copy a second portion of the boot code into volatile RAM. Once the second portion of the boot code is copied into RAM, the first portion of the boot code executes a branch (jump) instruction that transfers control to the second portion of the boot code that is in RAM. The second portion of the boot code

> is then able to take advantage of the random access nature of the RAM memory that allows for normal code execution, including jumps within the boot code in RAM. The second portion of the boot code is able to cause the appropriate commands to be sent to the sequential memory in order to transfer into RAM any other code that is needed.

Applicants amend claim 1 to specify, among other features, that the static random access memory ("SRAM") "continues to receive power even if said system is otherwise powered off, said SRAM thereby being available for use by the processor without needing to subsequently be initialized when the processor executes the initialization code." Claim 1 requires at least two memories: an initialization memory that contains initialization code and an SRAM that can be used to store variables during the execution of the initialization code. The SRAM is maintained in a state that permits the SRAM to be available for use during initialization without having to first be initialized. Gibson does not teach or suggest this combination of claim features. The Examiner seems to have analogized Gibson's sequential access memory 32 (also labeled as "Ultranand" in Figure 1) to the claimed SRAM. However, Gibson specifically teaches that the "memory 32 requires setup commands to be written to it before it is able to read data." Col. 3, lines 53-55. Gibson thus teaches that the memory 32 is not available for use until the memory 32 is initialized. Further, Gibson does not teach an apparatus that comprises the combination of a memory that contains executable initialization code and an SRAM that is available for use without subsequently being initialized to store variables while the initialization code is being executed. Claim 1 and its dependent claims are thus patentable at least for these reasons.

As noted above, the SRAM in claim 1 is used to "store variables used by the processor while executing said initialization code." Gibson does not teach or suggest that its memory 32 is capable of storing variables used by a processor during initialization. Gibson's memory 32 is an EEPROM and thus, as would be known by one of ordinary skill in the art, is not readily used as a storage location for variables used during execution of a program. Gibson's memory 32, instead,

is used for storing the boot code, which is flashed onto the EEPROM and is not variable.

At the bottom of page 2 of the Office Action, the Examiner noted that Gibson does not teach using an SRAM for a memory in which to store variables as claimed. The Examiner continues noting that SRAM is a type of volatile memory and Gibson allegedly teaches that "only volatile memory is used for this purpose." Applicants respectfully disagree. Gibson teaches that the memory 32 is a type of ROM (col. 3, lines 21-27) and not volatile memory as suggested by the Examiner. The purpose of the memory 32 in Gibson being a sequential access read only memory is to provide a permanent storage medium for the initialization code that is to be executed by the processor and in a memory that Gibson states has higher density and is cheaper than conventional ROMs. Applicants do not see why one of ordinary skill in the art would have been motivated to modify Gibson's sequential access memory with a volatile SRAM as suggested by the Examiner.

At the top of page 3 of the Office Action, the Examiner noted that Gibson does not teach separate memories as claimed. The Examiner notes that Gibson mentions the use of ROM and sequential access memory and, on that basis, concludes that "one of ordinary skill in the art would have readily recognized that using two separate memories (ROM and SRAM) is possible and applicable in Gibson's system." However, Gibson's invention is to **replace** the conventional ROM with sequential access memory. Thus, Gibson's teachings do not support the Examiner's contentions. For any or all of these reasons, Applicants submit that claim 1 and dependent claims 2-5 are allowable over Gibson.

Independent claim 6 is directed to a method that comprises, among other features, "providing power to said static random access memory even if the computer system is otherwise powered off" and "using the static random access memory to store and retrieve variables needed by the code without having to initialize the static random access memory." As explained above, Gibson does

not teach or suggest this combination of features. Accordingly, claim 6 and dependent claims 7-8 are allowable over Gibson.

Independent claim 9 is directed to a system that comprises "initialization memory containing initialization code" and "static random access memory...for storing variables for initializing the dynamic random access memory." Gibson does not teach or suggest that the memory 32 can be used to store variables for initializing anything, much less dynamic random access memory. At least for this reason, claim 9 and dependent claims 10-13 are allowable over Gibson.

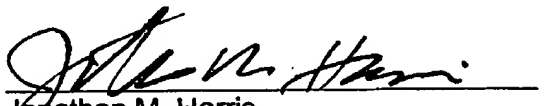
Independent claim 14 is directed to a system that comprises "static random access memory" that is "connected to and powered by a system power supply which remains active whenever AC power is supplied to the computer system." The Examiner contends that the Gibson's EEPROM 32 is akin to the claimed static random access memory. Gibson does not teach or even suggest that EEPROM 32 is "powered by a system power supply which remains active whenever AC power is supplied to the computer system." In addition, in claim 14 the static random access memory is "used to store variables used for initializing the dynamic random access memory while executing said initialization code." As explained above, Gibson does not teach or suggest this feature. For any or all of these reasons, claim 14 and dependent claims 15-16 are allowable over Gibson.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-

Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,



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